WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a pair of source/drain regions formed on the main surface of a silicon region at a prescribed interval to define a channel region and lifted up in an elevated structure;

a gate insulator film, formed on said channel region, consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9; and

a gate electrode including a first metal layer coming into contact with said gate insulator film and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions.

2. The semiconductor device according to claim 1, wherein

said source/drain regions include n-type source/drain regions, and

said gate electrode includes said first metal layer having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon.

3. The semiconductor device according to claim 2,

wherein

said first metal layer includes an Hf layer.

4. The semiconductor device according to claim 1, wherein

said source/drain regions include p-type source/drain regions, and

said gate electrode includes said first metal layer having said work function controlled to have a Fermi level around the energy level of the valence band of silicon.

5. The semiconductor device according to claim 4, wherein

said first metal layer includes either an Ni layer or an Ir layer.

6. The semiconductor device according to claim 1, wherein

said gate insulator film consisting of said high dielectric constant insulator film includes at least one film selected from a group consisting of an HfO_2 film, a ZrO_2 film and an HfAlO film.

7. The semiconductor device according to claim 1, wherein

said gate electrode includes:

said first metal layer having said controlled work function, and

a second metal layer, formed on said first metal layer, having a larger thickness than said first metal layer.

8. The semiconductor device according to claim 7, wherein

said second metal layer is a metal layer having an uncontrolled work function.

9. The semiconductor device according to claim 7, wherein

said second metal layer includes at least either a TaN layer or a TiN layer.

10. The semiconductor device according to claim 7, wherein

said first metal layer is formed in a U shape, and

said second metal layer is formed to fill up a region enclosed with the U-shaped portion of said first metal layer.

11. The semiconductor device according to claim 1,

further comprising source/drain electrodes, formed on the upper surfaces of said pair of source/drain regions having the elevated structure to be in contact with the upper surfaces of said pair of source/drain regions without interposition of metal silicide films, including third metal layers having a work function controlled to have a Fermi level around the energy level of the band gap end of silicon constituting said source/drain regions.

12. The semiconductor device according to claim 11, wherein

said source/drain regions include n-type source/drain regions, and

said source/drain electrodes include said third metal layers having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon.

13. The semiconductor device according to claim 12, wherein

said third metal layers include Hf layers.

14. The semiconductor device according to claim 11, wherein

said source/drain regions include p-type source/drain

regions, and

said source/drain electrodes include said third metal layers having said work function controlled to have a Fermi level around the energy level of the valence band of silicon.

15. The semiconductor device according to claim 14, wherein

said third metal layers include either Ni layers or Ir layers.

16. The semiconductor device according to claim 11, wherein

said pair of source/drain regions having the elevated structure include:

said third metal layers having said controlled work function, and

fourth metal layers, formed on said third metal layers, having a larger thickness than said third metal layers.

17. The semiconductor device according to claim 16, wherein

said fourth metal layers are metal layers having an uncontrolled work function.

18. The semiconductor device according to claim 16, wherein

said fourth metal layers include at least either TaN layers or TiN layers.

19. The semiconductor device according to claim 1, wherein

said silicon region includes a silicon layer formed on an insulator.

20. The semiconductor device according to claim 19, further comprising element isolation insulator films formed on the outer sides of said pair of source/drain regions having the elevated structure to reach said insulator.

21. A semiconductor device comprising:

a pair of source/drain regions formed on the main surface of a silicon region at a prescribed interval to define a channel region;

a gate insulator film, formed on said channel region, consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9;

a gate electrode, formed on said gate insulator film,

including a metal layer coming into contact with said gate insulator film; and

source/drain electrodes, formed on the upper surfaces of said pair of source/drain regions to be in contact with the upper surfaces of said pair of source/drain regions without interposition of metal silicide films, including metal layers having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions.

22. The semiconductor device according to claim 21, wherein

said source/drain regions include n-type source/drain regions, and

said source/drain electrodes include said metal layers having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon.

23. The semiconductor device according to claim 22, wherein

said metal layers include Hf layers.

24. The semiconductor device according to claim 21, wherein

said source/drain regions include p-type source/drain regions, and

said source/drain electrodes include said metal layers having said work function controlled to have a Fermi level around the energy level of the valence band of silicon.

25. The semiconductor device according to claim 24, wherein

said metal layers include either Ni layers or Ir layers.